# Analysis of a MOSFET operating as an RF power detector

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***Abstract*—This paper presents the analysis of a MOSFET biased in the triode region operating as a power detector. Two modes of operation are evaluated, current mode and voltage mode. For each mode, we develop expressions relating a DC signal and the squared amplitude of a RF signal. A MOSFET compact model, valid for any inversion level, is used, permitting to predict the detector behavior with a reasonable accuracy. Optimization of the CMOS power detector is discussed remarking the trade-off between sensor's sensitivity and input impedance. The approach is validated through simulations and measurements results, which present good agreement with the theory.**

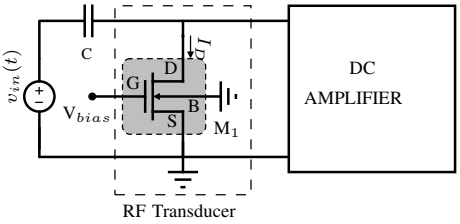


Fig. 1. Behavioral model of the power transducer

## I. Introduction

In the technical literature different ways to implement power detectors for BIT (Built-in-test) are presented. Some of them are based on the nonlinearity of devices such as Schottky diodes, which are used to rectify the input signal and to generate a DC signal proportional to the squared amplitude of the RF signal [1]. Another approach uses bipolar transistors [2], where the translinear principle is employed to produce a DC output proportional to the RF input power. Integrated CMOS sensors using the nonlinear behavior of a NMOS transistor biased in the triode region are adopted in [3]–[5]. These works have in common the use of CMOS technology, a necessary condition to design BIT in SoC . Nevertheless, the authors do not offer a complete analysis of the MOSFET sensor, offering no means to the designer for extracting the best performance of the transducer, which depends mainly on the component dimensions and DC operating point.

In this work, we consider a power sensor as the one depicted in Fig. 1, which comprises a MOSFET transducer and a DC amplifier. In such a circuit, the designer has the choice of using a voltage or a current DC amplifier. For both approaches, expressiones are developed relating the generated DC current (current mode technique) or DC voltage (voltage mode technique) and the RF signal. The expressions are based on a MOSFET compact model valid for any inversion level, which offer great insight for the designer. Simulations and measurements are realized in order to validate the theoretical analysis. From the observations, we can conclude that a sensor of dimensions of $150/1.25$ $\mu$m/$\mu$m can deliver a current of about $0.1$ $\mu$A for a $10$ mV RF signal, when biased at an inversion level of 10. In addition, the sensor's impedance can be designed for matching a typical $50$ $\Omega$ source, by choosing its dimensions and further tuning its operating point.

This paper is organized as follows: after this introduction, we review the MOSFET compact model and develop the sensor model in Section II. Then, in Section III, we show a comparison between theoretical and simulation results. Section IV is dedicated to presenting measurement results and finally, in Section V some discussions and conclusion are drawn.

## II. The MOSFET as a RF power-to-DC current transducer

A MOSFET is a four terminal device which can be used as a nonlinear controlled resistor. Different MOSFET compact models have been developed in the last two decades, some based on the surface potential (PSP) [6], others, on the inversion charge (ACM, EKV) [7], [8]. In this work, the ACM model is chosen to described the MOSFET I-V characteristic, leaving open the development using the others models. When a RF voltage signal is applied between the MOSFET drain and source terminals, a harmonic-rich current flows through the device's channel, whose intensity is mainly dependent on the transistor's dimensions and on the forward ($i_f$) and reverse ($i_r$) inversion levels, controlled by the gate potential. For small RF signals, the DC component of the current is proportional to the square of the RF signal amplitude. So, by measuring this DC current, we can estimate the power of the RF signal.

There are two possible techniques to measure the DC current; both dependent on the DC impedance of the measurement circuit connected to the MOSFET. A low DC impedance means to use current mode technique to sense the RF power, whereas a high DC impedance is related to a voltage mode technique.

### A. Review of the quasi-static MOSFET model

The MOSFET inversion levels (forward and reverse) can be described by the expressions below (neglecting short-channel effects[1]) [7]:

$$\frac{V_P - V_{S(D)}}{\phi_t} = \sqrt{i_{f(r)} + 1} - 2 + \ln\left(\sqrt{i_{f(r)} + 1} - 1\right) \quad (1)$$

$$\frac{V_P - V_{S(D)}}{\phi_t} = F\left(i_{f(r)}\right) \quad (2)$$

where $V_P$ is the channel pinch-off voltage, which is a function of the gate potential $V_G$, $V_{S(D)}$ is the voltage at source (drain) terminal, and $\phi_t$ is the thermal voltage. All voltages are measured with respect to the bulk volatge. The explicit relationship between the terminal voltages and the inversion levels is given by:

$$i_{f(r)} = 2W_0\left\{\alpha_{f(r)}\right\} + W_0^2\left\{\alpha_{f(r)}\right\} \quad (3)$$

$$\alpha_{f(r)} = \exp\left(\frac{V_P - V_{S(D)}}{\phi_t} + 1\right) \quad (4)$$

where $W_0\{\cdot\}$ is the Lambert (omega) function [9].

The drain current is obtained from:

$$I_D = I_F - I_R = I_{SH} S(i_f - i_r) \quad (5)$$

where $I_{F(R)}$ are the forward(reverse) currents, $I_{SH}$ is the sheet normalization current, which depends on technological parameters, $W$ is the transistor width and $L$ its channel length. The ratio between $W$ and $L$ is the transistor aspect ratio $S = W/L$. After reviewing the fundamental equations of the MOSFET charge-based model, we are able to find an expression for the average component of the transistor current.

### B. Expression for the transducer operating in current mode

Considering a MOSFET sensor configured as in Fig. 1, for a RF input signal of magnitude $V_{RF}$ and frequency $f = 1/T$, the drain voltage can be expressed as $v_D(t) = V_D + V_{RF}\cos\left(\frac{2\pi}{T}t\right)$, where $V_D$ is the drain DC voltage. The DC current flowing through the transistor's channel, for any level of signal, can be estimated by:

$$I_{DC} = \frac{1}{T}\int_0^T I_D(t)\,dt = I_F - \frac{S}{T} I_{SH}\int_0^T i_r(t)\,dt \quad (6)$$

where $I_D(t)$ is the drain current, which is dependent on $v_D(t)$. $I_F$ is constant in (6), since it is related to the forward inversion level, which is fixed by $V_{bias}$ and $V_S$ (0 V in the circuit of Figure 1). The second term, associated with $i_r$, is variable and depends on the voltage at the drain terminal. Particularly, due to $W_0\{\cdot\}$ being a monotonic increasing function, $I_{DC}$ is negative for $V_D = 0$, indicating a DC current flowing from the source to the drain terminal.

[1]Since the transistor operates in deep triode, short-channel effects are irrelevant, except the mobility degradation due to changes in the vertical field with $V_{GS}$.

Evaluating (6) can be cumbersome, so an approximate expression for weak signals is obtained considering the Taylor series of the current, neglecting memory effects. In this case, the current $I_D(t)$ can be expanded in a power series on $v_{in}$ as:

$$I_D(t) = \sum_{n=1}^{\infty} \frac{a_n}{n!} v_{in}^n(t) \qquad a_n = \left.\frac{\partial^n I_D(t)}{\partial v_{in}(t)^n}\right|_{i_f, i_{rQ}} \quad (7)$$

where $i_{rQ}$ is obtained from (3) for given $i_f$ and $V_D$ voltage, recalling that if $V_D$ is zero the value of $i_{rQ}$ equals $i_f$.

For weak signals, where the contribution of the even high order terms to the DC current can be neglected, the evaluation of (7) results in a current which average value is linearly related to the magnitude squared of the input signal, given by:

$$I_{DC} \simeq \frac{1}{T}\int_0^T \frac{a_2}{2} v_{in}^2(t)dt \quad (8)$$

$$I_{DC} \simeq -\frac{I_{SH} S}{2\phi_t^2}\left(\frac{\sqrt{i_{rQ}+1} - 1}{\sqrt{i_{rQ}+1}}\right) V_{RF}^2 \quad (9)$$

In (8), the proportionality coefficient $a_2$ can also be interpreted as the first derivate of the drain transconductance ($g_{md}$) [7], which increases linearly with the aspect ratio ($S$) and depends on the reverse inversion level at the bias condition $i_{rQ}$. Even though the maximum current for a given input power is obtained for $i_{rQ}$ tending to infinity, 90% of the maximum current can be measured for values of $i_{rQ}$ of the order of 100. Due to the fact that the sensor has no power consumption and has a well defined sensitivity when $V_D = 0$ ($i_{rQ} = i_f$), this is the ideal operating point for this application.

### C. Expression for the transducer operating in voltage mode

When there is no path for transistor's DC current a constant voltage $V_{DC}$ appears at the transistor drain to force $I_{DC} = 0$. Using (2), we can write the drain-source average voltage as,

$$V_{DC} = \frac{\phi_t}{T}\int_0^T \left\{F\left(i_f\right) - F\left(i_r\right)\right\} dt \quad (10)$$

Recalling that $i_f$ is constant, the term $F\left(i_f\right)$ is also constant. However, $F\left(i_r\right)$ is difficult to evaluate explicitly because the reverse inversion level depends on the $V_{DC}$ and $V_{RF}$ voltages. Nevertheless, by making $I_{DC} = 0$ in (6), the expression $i_f = \overline{i_r}$ is obtained and $V_{DC}$ is infered from,

$$i_f = \frac{1}{T}\int_0^T i_r\left\{(v_D(t)\right\} dt \quad (11)$$

For weak input signals, the voltage at the transistor's drain is obtained by applying the Ohm's law to the MOSFET. So, the product between (9) and transistor's drain transconductance [7] gives:

$$V_{DC} \simeq \frac{V_{RF}^2}{4\phi_t\sqrt{i_{rQ}+1}} \quad (12)$$

The result is an expression relating a constant voltage between the drain-source voltage and the square of the input

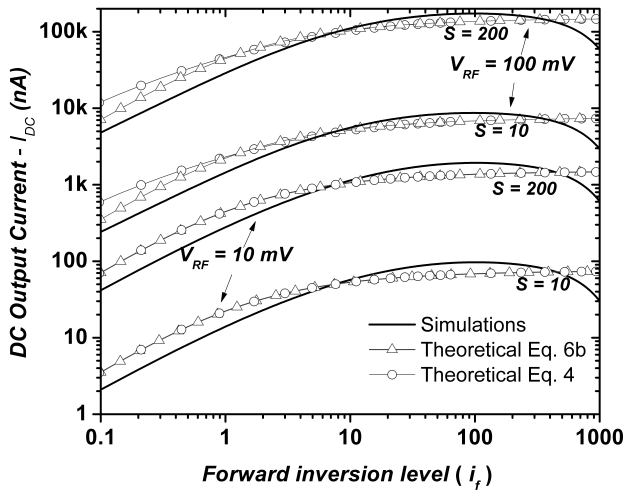


Fig. 2. DC output current ($I_{DC}$) according to (6), (9) and harmonic balance simulation in ADS, for $V_D = 0$, $V_{RF} = \{10, 100\}$ mV.

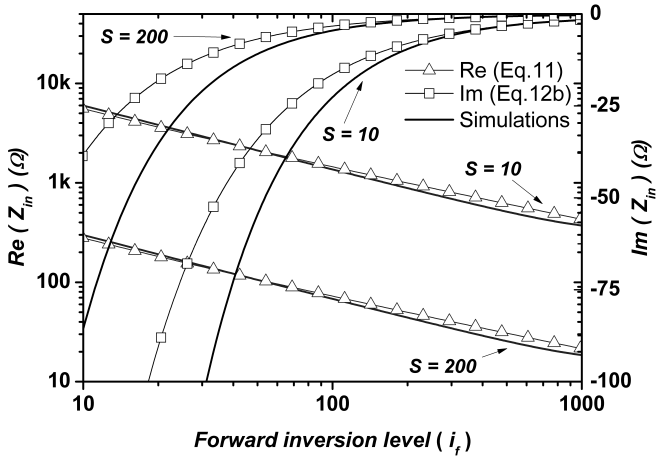


Fig. 3. Real and imaginary part of the input impedance $Z_{in}$, theoretical and simulated values at 2.4 GHz, for $V_D = 0$, as a function of the forward inversion level for two different aspect ratio ($S = \{10, 200\}$).

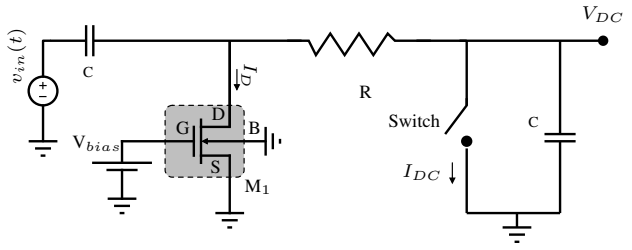


Fig. 4. Discrete Circuit Schematic for power sensor (current and voltage mode operation) measurements.

signal amplitude. Some characteristics of (12) are: a) considering no DC current flowing through the transistor, the drain voltage is always positive since the nonlinearity of the transistor would impose a negative DC current when a RF input signal is present; b) it saturates for low values of $i_f$ (weak inversion: $i_f < 1$) and has no dependence on the aspect ratio, being this fact a remarkable difference with respect to the current mode previously discussed.

### *D. MOSFET power detector input impedance*

Applying the non-quasistatic model of the MOS transistor [10], the input impedance $Z_{in}$ seen from the drain can be expressed as,

$$Z_{in} = \left[g_{md} + j\omega C_{dd}\right]^{-1} \tag{13}$$

$$g_{md} = \frac{2I_{SH}S}{\phi_t}\left(\sqrt{i_{rQ}+1}-1\right) \tag{14}$$

$$C_{dd} = C_{bd} + C_{sd} + C_{gd} \tag{15}$$

$$C_{dd} = \frac{nC_{ox}^{'}SL^2}{3}\left(\frac{\sqrt{i_{rQ}+1}-1}{\sqrt{i_{rQ}+1}}\right) \tag{16}$$

The transconductance and the capacitance are proportional to the aspect ratio, but the dependency on the reverse inversion coefficient is different. While the former increases with the inversion coefficient, the latter tends to a constant value.

## III. Simulation results

In this section, the previous analysis is validated with ADS Agilent® simulations. We designed a MOSFET sensor in a $0.18\,\mu$m process, with a $I_{SH} = 95$ nA, extracted using the methodology described in [7]. For evaluating the sensor in current mode, we excited the transistor with a zero average 2.4 GHz voltage signal and varied the bias point ($i_f$) from 0.1 to 1000 for several aspect ratios ($S$). The results are plotted in Fig. 2, from which we can observe the simulation values following the predicted ones, with a few discrepancies that are accentuated at the extremities. The disagreement could be explained by noticing that both the mobility ($\mu_n$) and the slope factor ($n$) are dependent on the operating point [7]. It is important to notice that the current is maximum in the transition from moderate to strong inversion ($i_f \simeq 100$), due to the $a_2$ saturation and the $I_{SH}$ degradation. In addition, we can remark from the curves, that the current is proportional to the aspect ratio, as expected, and no significant differences are detected between (6) and (9) for $V_{RF}$ values up to 100 mV.

We also evaluated the behavior of the small-signal impedance of the sensor. For estimating $C_{dd}$, the oxide capacitance per area ($C_{ox}^{'}$) was obtained from the oxide thickness of the technology. In Fig. 3, we summarize the results obtained from ADS simulations against the evaluation of (13). The real and imaginary parts of $Z_{in}$ are plotted as function of the inversion level and the aspect ratio. From the curves we recognize that the real part decreases when either the aspect ratio or the inversion level increases. This behavior is an interesting feature for impedance tuning. First, a coarse impedance value can be determined by choosing the transistor dimensions at the design phase and further, during operation, it can be fine-tuned adjusting the bias point. We also can distinguish that the imaginary part is always lower than the real part, reaching values below $1\Omega$ in strong inversion. A $50\Omega$ resistive input impedance can be easily obtained, without

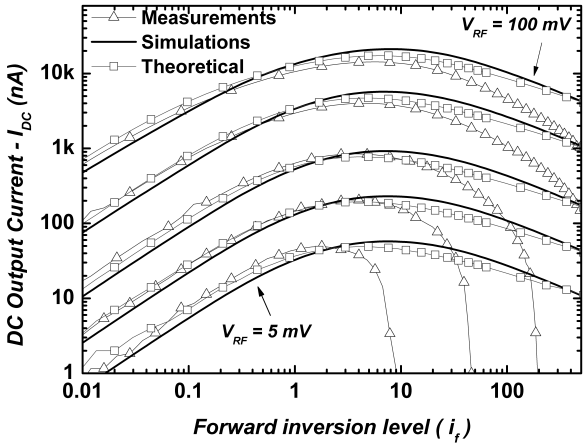


Fig. 5. Output DC current ($I_{DC}$) according to (6), ADS harmonic balance simulation and measurements, as a function of the operating point ($i_f$) for different input amplitudes [$V_{RF}(mV) = \{5, 10, 20, 50\ and\ 100\}$].

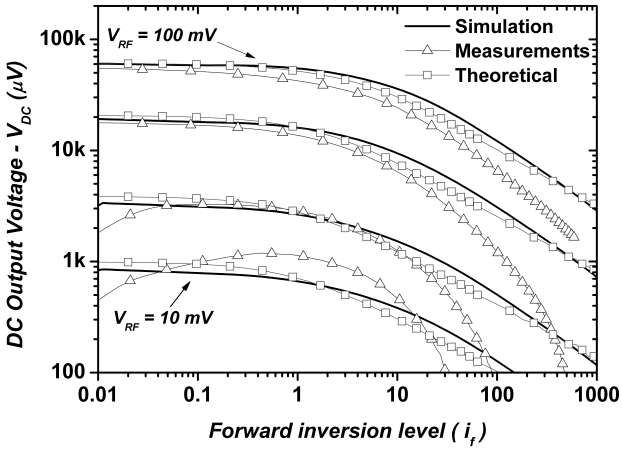


Fig. 6. Output DC voltage ($V_{DC}$) according to (11), ADS harmonic balance simulation and measurements, as a function of the operating point ($i_f$) for different input amplitudes [$V_{RF}(mV) = \{10, 20, 50\ and\ 100\}$].

inductor compensation, for a transistor with S = 200, biased at $i_f = 200$.

## IV. Measurement results

The circuit of Fig. 4 was assembled for verifying the proposed model at the two operating modes. The voltage mode could be evaluated by opening the switch, avoiding a DC path for the current, whereas the current mode was selected by closing the switch. Even though the resistor $R$ induces a DC voltage on the drain terminal, its value ($1\ k\Omega$) was chosen so that the product $R \cdot I_{DC}$ is negligible. The transistor used has an aspect ratio of 125 (L = 1.2 $\mu$m and W = 150 $\mu$m), on a 0.35 $\mu$m technology, with $I_{SH} = 62$ nA. The frequency of the RF signal was set at 10 MHz and the capacitor ($C$) value was 470 nF. The measurements were taken from a semiconductor parameter analyzer 4156 from Agilent ®.

In Fig. 5 and 6, measurements, simulation and theoretical results are presented. The sensor's DC current and DC voltage are plotted against the forward inversion level for different amplitudes of the RF signal. Measurements show good agreement in weak inversion ($i_f < 10$), however, in the moderate region, both, DC current and DC voltage decrease quicker than the simulated and the theoretical values. This behaivour is due to imperfections in the measurement setup circuit, specially, to the voltage difference between the transistor source and load resistor (R), which are connected to different Agilent ® 4156's source measure units. With the increasing inversion level value, the resistence seen by this two nodes is dominated by the load resistor. A voltage difference of 100 $\mu$V will give a current of 100 nA counteracting the DC current generated by the RF input signal. In Fig. 5 is shown that almost the same current is subtracted from each measured current, canceling it for low RF siganls values.

## V. Conclusion

A detailed analysis of the CMOS power detector presented in [3] is developed. Expressions for the sensitivity from low to high input signal power are obtained and compared with simulated and measured values in two different technologies. The behavior of the input impedance with the aspect ratio and inversion level values is studied, emphasizing the trade-off between sensitivity and input impedance, showing the versatility of the design variables which allows power detector designs for different applications.

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