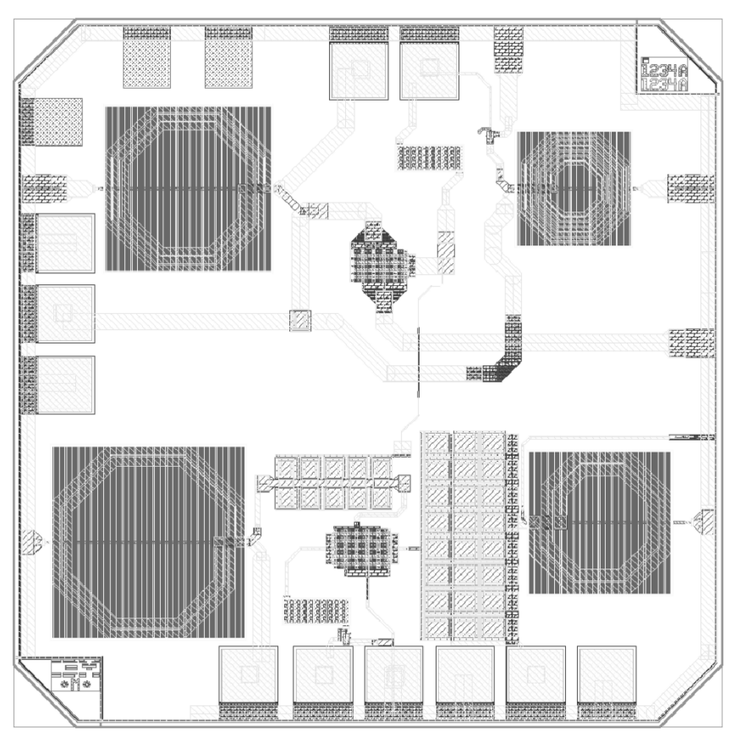
UFSC
Radio Frequency Integrated Circuits
Research Group – GRF
Federal University of Santa Catarina
Florianópolis – SC, Brazil
floripa design house

A 2.4 GHz Fully-Integrated CMOS Class-AB Power Amplifier

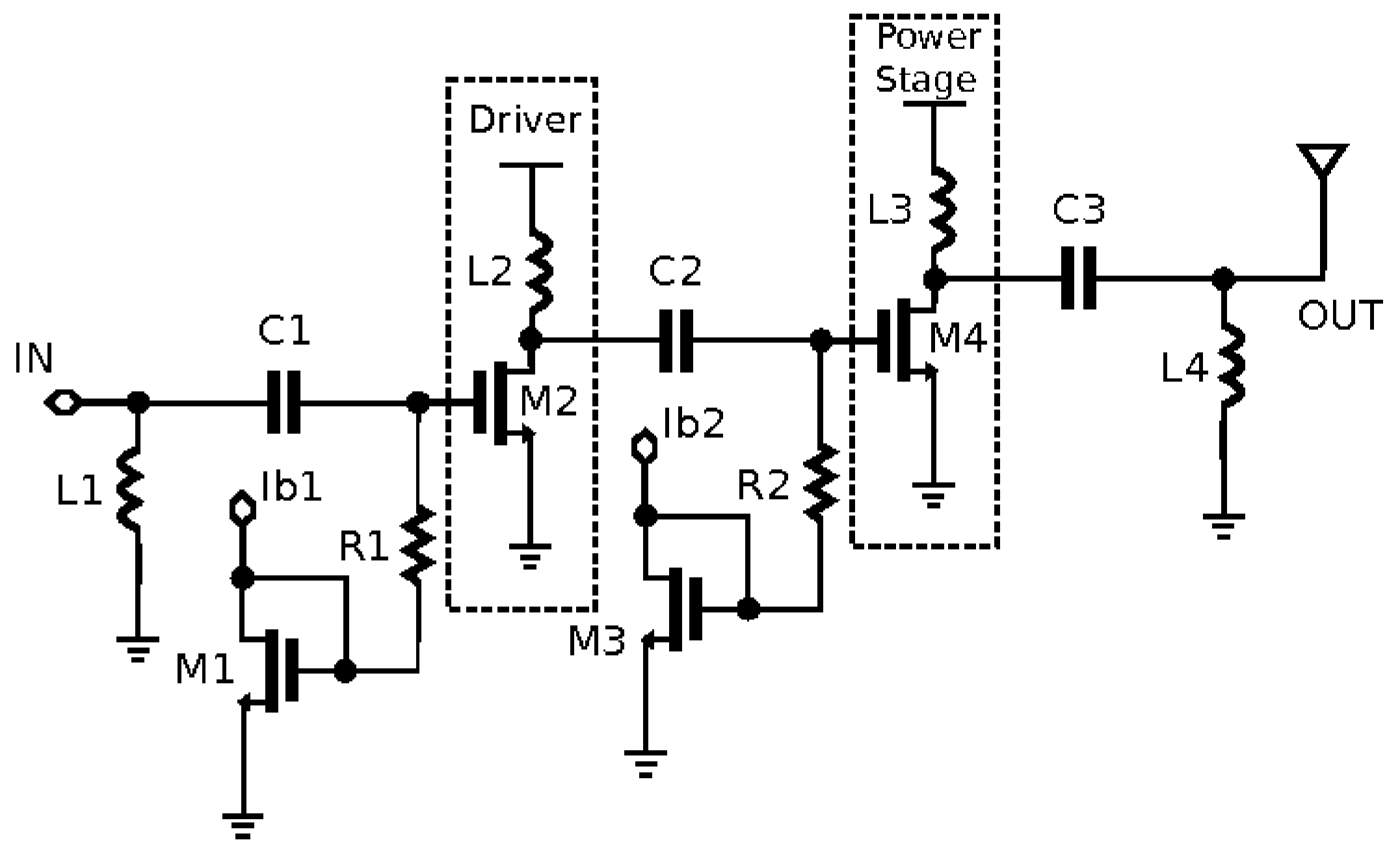
M. B. Moreira , F. R. de Sousa
mateus.moreira@floripadh.com



Abstract

A Class-AB 2.4 GHz Power Amplifier (PA) is presented in this paper. The input stage is an input driver and the second stage is the power core. The components were integrated on the same chip in a 0.18-μm CMOS process.The simulation results show that the PA achieves high power gain of 23dB with output power of 12.45dBm and drain efficiency of 41 %.

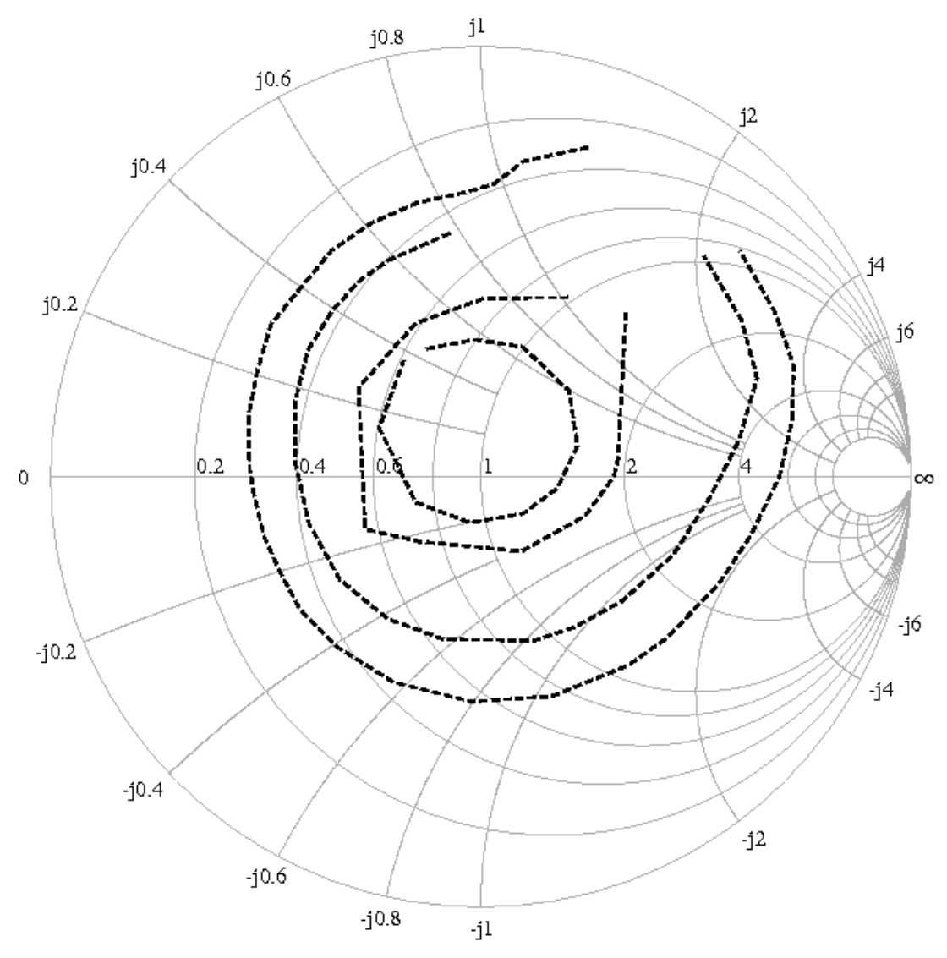
Proposed Topology



The presented PA consists of dual stage amplifier including input and output matching networks. The input matching network provides a 50 matching at 2.4 GHz between the driver and the source. This matching is performed to facilitate future measurements since it is necessary to identify the amount of power delivered by the source. The output matching network is designed to provide the optimum impedance to the power stage in order to achieve the highest output power at the antenna.

Design Methodology

Load-Pull



The Load-Pull Characterization is performed by measuring the amount of mismatch which may exist between the amplifier and the load to deliver the highest power. For this purpose the magnitude and phase of reflection coefficient between amplifier and the load are swept by simulation. Hence, the optimum impedance for the load is obtained from power contours plots on the Smith chart.

Stability

$$K = \frac{1-|S_{11}|^2-|S_{22}|^2+|\Delta|^2}{2|S_{12}S_{21}|}$$

$$\beta_{1f} = 1+|S_{11}|^2-|S_{22}|^2-|\Delta|^2$$

$$\Delta = S_{11}S_{22}-S_{12}S_{21}$$

In order to have an unconditionally stable amplifier this analysis must result in $K > 1$ and $\beta_{1f} > 0$.

Drain Efficiency

Some research works presented the efficiency of PA as Power added efficiency. In this work the metric used is the drain efficiency.

$$Drain\ Efficiency = \frac{\mathrm{P_{load}}}{P_{DC}}$$

Simulation Results

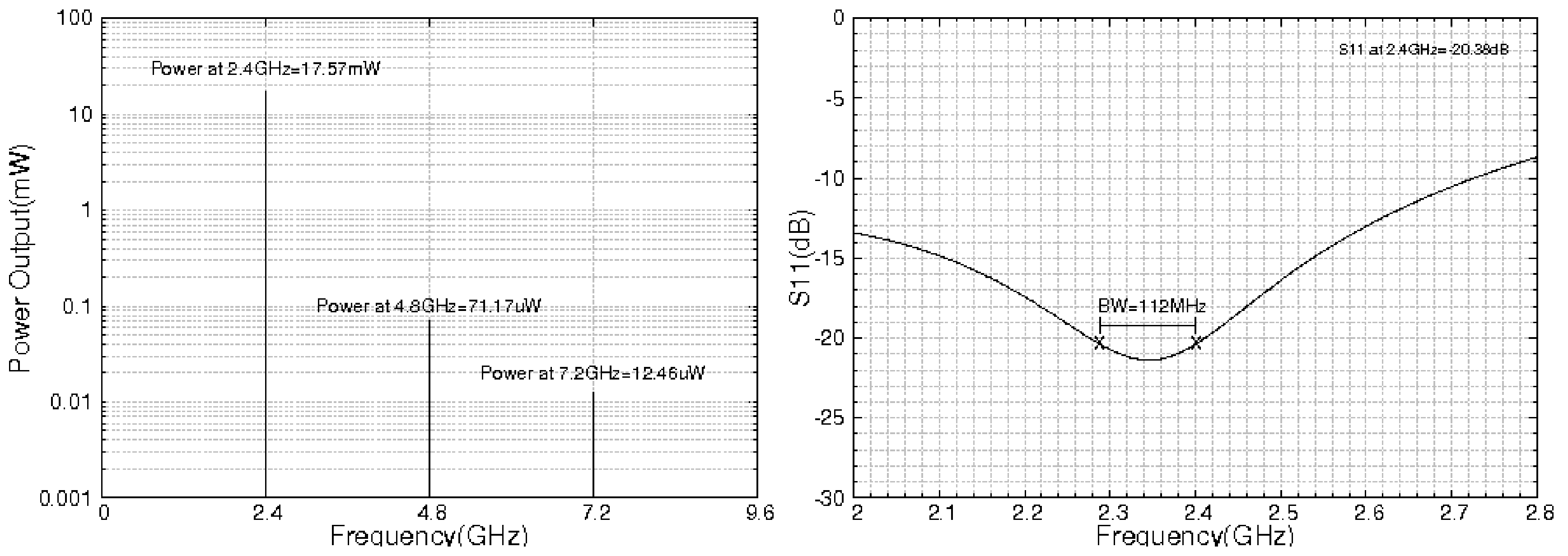


Figure 1: Spectrum of output power

Figure 2: Input Reflection Coefficient (S_{11})

Table 1: MoteCarlo Analysis

	σ	μ	N
Output Power	1.73mW	17.35mW	442
Power Consumption	1.64mW	41.92mW	442
K	0.032	1.70	442
β_{1f}	0.004	0.85	442
S_{11}	1.03dB	-20.27dB	442
Efficiency	2.67%	41.4%	442

Table 1: Corners Analysis

Corner	Output Power (mW)	DC Consumption (mW)	K	β_{1f}	S_{11} (dB)	Efficiency (%)
Nominal	17.57	42.08	1.7	0.856	-20.38	41.75
ff	21.64	46.02	1.652	0.856	-22.09	47.02
ss	13	37.53	1.765	0.855	-18.75	34.63
fff	23.03	47.4	1.638	0.855	-22.8	48.58
ssf	12.03	36.57	1.779	0.855	-18.42	32.89

References

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